AMENDMENTS TO THE DRAWINGS:

The attached two (2) replacement sheets of amended drawings (Figures 1-4), include changes to Figures 1-3. These replacement sheets have been amended to include the term "PRIOR ART" with reference to Figures 1-3, and are submitted to replace the original sheets including Figures 1-4.

Attachment: Replacement Sheets (Figures 1-4).

REMARKS

Applicants have now had an opportunity to carefully consider the Examiner's comments set forth in the Office Action of February 23, 2007.

Reconsideration and allowance of the subject application are respectfully requested.

Claims 1 and 2 have been amended. New Claims 13 to 15 have been added. Claims 1 to 15 are now pending in the application. Claim 8 has been withdrawn as being drawn to a non-elected species. Claim 1 is independent.

In the Official Action, the Examiner has requested that Figures 1 to 5 be designated by the "Prior Art" legend. The Examiner's request is appropriate only for Figures 1 to 3. Replacement Figures 1 to 3 with the "Prior Art" legend are being submitted concurrently herewith. Contrary to the Examiner's allegation, Figures 4 and 5 do not show that which is old.

The specification has been amended to correct the typographical error noted by the Examiner on page 10 as well as to correct other clerical errors noted by the Applicant.

The Examiner has rejected claims 1 to 7 and 9 to 12 under 35 U.S.C. §112, second paragraph. The Examiner is alleging that use of the term "thick" in claim 1 and the use of the phrase "conforms generally" in claim 2 renders these claims indefinite. With respect to the Examiner's objection for use of the term "thick", Applicant respectfully submits that the Examiner's objection is inappropriate. U.S. Patent Application No. 09/504,472 (now U.S. Patent No. 6,448,950) incorporated by reference in the subject application provides the standard for ascertaining the requisite degree to enable one of ordinary skill in the art to be reasonably apprised of the scope of the claimed invention. Further, at least column 6, lines 27-54, clearly shows the meaning of this term in the present technology is understood by one of ordinary skill in the art. Accordingly, Applicant respectfully requests that this objection be removed. Claim 2 has been amended to remove the term "generally" to address the Examiner's objection.

With respect to prior art, the Examiner has rejected claims 1 to 7 and 9 to 12 under 35 §U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,417, 825 to Stewart et al. ("Stewart"). Applicant respectfully submits that the Examiner's objection in view of

the cited reference is no longer appropriate.

According to the Applicant's invention as defined by independent claim 1, Applicant provides a gray scale column driver for a thick dielectric electroluminescent display. The gray scale column driver comprises a counter receiving gray level data from an incoming video signal and in response counting for a time interval proportional to the gray level data. A non linear voltage ramp generator is connected to the counter. The non linear voltage ramp generator outputs a ramping voltage for application to columns of the display during the time interval. The ramping voltage, between its start and peak, conforms to a curve having an inverted s-shape, with an initial convex portion followed by a concave portion so as to compensate for luminance versus voltage characteristics of the thick dielectric electroluminescent display.

In contrast, Stewart discloses an active matrix electroluminescent display (AMEL display) that produces gray scale operation comprising an array of pixels, each pixel including a first transistor having its gate connected to a select line, its source connected to a data line, and its drain connected to the gate of a second transistor. The second transistor has its source adapted to receive a ramped voltage level, and its drain connected to a first electrode of an electroluminescent cell. The electroluminescent cell has a second electrode connected to an alternating current, high voltage power source. The electroluminescent cell is illuminated when the ramp voltage level is less than a voltage level on the gate of the second transistor. The ramp voltage level is increased linearly during a frame duration, and the alternating current, high voltage power source is on continuously during the same frame duration. The alternating current, high voltage power source may also be varied in amplitude from a minimum peak-to-peak value to a maximum peak-to-peak value during the frame duration.

As the Examiner will appreciate from the description and Figures of Stewart, the ramp voltage is **LINEAR** between its start and peak. In no way does Stewart hint at, suggest or teach a ramping voltage that, ***between its start and peak, conforms to a curve having an inverted s-shape, with an initial convex portion followed by a concave portion*** so as to compensate for luminance versus voltage characteristics of the thick dielectric electroluminescent display. Accordingly, Applicant respectfully

submits that independent claim 1 and the claims dependent thereon distinguish patentably over the cited prior art and should be allowed.

In view of the above, it is believed the application is in order for allowance and action to that end is respectfully requested.

CONCLUSION

For the reasons detailed above, it is submitted all claims remaining in the application (Claims 1-7 and 9-15) are now in condition for allowance. The foregoing comments do not require unnecessary additional search or examination.

In the event the Examiner considers personal contact advantageous to the disposition of this case, he/she is hereby authorized to call Mark S. Svat, at Telephone Number (216) 861-5582.

Respectfully submitted,

FAY SHARPE LLP

8/23/07
Date

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METHOD AND APPARATUS FOR GRAY-SCALE GAMMA CORRECTION FOR ELECTROLUMINESCENT DISPLAYS

FIELD OF THE INVENTION

The present invention relates generally to flat panel displays, and more particularly to a method and apparatus for driving a display panel requiring gray scale control by modulation of the voltage applied to the column electrodes with a non-linear voltage ramp.

BRIEF DESCRIPTION OF THE DRAWINGS

The Background of the Invention and Detailed Description of the Preferred Embodiment are set forth herein below with reference to the following drawings, in which:

~~Fig.~~ Figure 1 is a plan view of an arrangement of rows and columns of pixels of an electroluminescent display, in accordance with the Prior Art;

~~Fig.~~ Figure 2 is a cross section through a single pixel of the electroluminescent display of Figure 1;

~~Fig.~~ Figure 3 is a luminance versus applied voltage curve for the electroluminescent pixel of Figure 1;

~~Fig.~~ Figure 4 shows voltage ramp curves for a negative row voltage and for a positive row voltage to generate gray scale luminance from the luminance versus voltage curve of Figure 3;

~~Fig.~~ Figure 5 shows a stepwise linear approximation of the Gamma correction curve of ~~Fig~~ Figure 4;

~~Fig.~~ Figure 6 is a block diagram of a non-linear ramp generator for Gamma correction

according to the preferred embodiment;

~~Fig.~~ Figure 7 is a schematic circuit diagram for a successful prototype of the non-linear ramp generator of Figure 6; and

~~Fig.~~ Figure 8 shows luminance versus gray level curves for a 17 inch thick dielectric electroluminescent display both using the Gamma correction circuit of Figure 7 and without using the Gamma correction circuit.

BACKGROUND OF THE INVENTION

Electroluminescent displays are advantageous by virtue of their low operating voltage with respect to cathode ray tubes, their superior image quality, wide viewing angle and fast response time over liquid crystal displays, and their superior gray scale capability and thinner profile than plasma display panels.

As shown in Figures 1 and 2, an electroluminescent display has two intersecting sets of parallel electrically conductive address lines called rows (ROW 1, ROW 2, etc.) and columns (COL 1, COL 2, etc.) that are disposed on either side of a phosphor film encapsulated between two dielectric films. A pixel is defined as the intersection point between a row and a column. Thus, Figure 2 is a cross-sectional view through the pixel at the intersection of ROW 4 and COL 4, in Figure 1. Each pixel is illuminated by the application of a voltage across the intersection of row and column defining the pixel.

Matrix addressing entails applying a voltage below the threshold voltage to a row while simultaneously applying a modulation voltage of the opposite polarity to each column that bisects that row. The voltages on the row and the column are summed to give a total voltage in accordance with the illumination desired on the respective sub-pixels, thereby generating one line of the image. An alternate scheme is to apply the maximum sub-pixel voltage to the row and apply a modulation voltage of the same polarity to the columns. The magnitude of the modulation voltage is up to the difference between the maximum voltage

and the threshold voltage to set the pixel voltages in accordance with the desired image. In either case, once each row is addressed, another row is addressed in a similar manner until all of the rows have been addressed. Rows that are not addressed are left at open circuit.

The sequential addressing of all rows constitutes a complete frame. Typically, a new frame is addressed at least about 50 times per second to generate what appears to the human eye as a flicker-free video image.

In order to generate realistic video images with flat panel displays, it is important to provide the required luminosity ratios between gray levels where the driving voltage is regulated to facilitate gray scale control. This is particularly true for electroluminescent displays where gray scale control is exercised through control of the output voltage on the column drivers for the display.

Traditional thin film electroluminescent displays employing thin dielectric layers that sandwich a phosphor film interposed between driving electrodes are not amenable to gray scale control through modulation of the column voltage, due to the very abrupt and non-linear nature of the luminance turn-on as the driving voltage is increased. By way of contrast, electroluminescent displays employing thick, high dielectric, constant dielectric layered pixels have a nearly linear dependence ~~of~~ on the luminance above the threshold voltage, and are thus more amenable to gray scale control by voltage modulation. However, even in this case if the gray scale voltage levels are generated by equally spaced voltage levels then the luminance values of the gray levels are not in the correct ratios for video applications.

The gray level information in a video signal is digitally encoded as an 8 bit number. These digitally coded gray levels are used to generate reference voltage levels V_g that facilitate the generation of luminance levels (Lg) for each gray level in accordance with an empirical relationship of the form:

$$Lg = f(V_g) = A\, n^{\gamma} \quad \text{(Equation 1)}$$

where $f(V_g)$ represents that the luminance is a function of the voltage applied to a pixel and A is a constant, n is the gray level number and γ is typically between 2 and [[.]] 2.5.

An electroluminescent (EL) display driver with gray scale capability resembles a digital-to analog (D/A) device with an output buffer. The purpose is to convert incoming gray scale 8-bit digital data from the video source to an analog output voltage for panel driving. There are various types of gray scale drivers, each ~~employs~~ employing a different method of performing the necessary digital-to-analog conversion. The present invention is related to the type of gray scale drivers that use a linear ramping voltage as a means of performing the D/A conversion. For this type of ~~drivers~~ driver, the digital gray level code is first converted to a pulse-width through a counter operated by a fixed frequency clock. The time duration of this pulse-width is a representation of, and corresponds to, the gray level digital code. The pulse-width output of the counter controls a capacitor sample-and-hold circuit which operates in conjunction with an externally generated linear voltage ramp to achieve the pulse-width to voltage conversion. Since the linear ramp has a linear relationship between the output voltage and time, the pulse-width representation of the digital code therefore generates a linear gray level voltage at the driver output. The luminance created for each level is then dependent on the relationship between the voltage applied to a pixel and the pixel luminance, which is the basic electro-optical characteristic of the particular panel. This luminance-voltage characteristic is normally different from the ideal characteristic, and therefore Gamma correction is necessary.

The relationship between the voltage applied to a pixel and its luminance is typified by the curve in Figure 3. The luminance begins to rise above the threshold voltage in a nonlinear fashion for the first few volts above the threshold, and then rises in an approximate linear fashion before saturating at a fixed luminance. The portion of the curve used for display operation is the initially rising portion and the linear portion. The effects of differential loading of the driver outputs complicate the relationship. To negate the effect of variable loading and to improve the energy efficiency of the display, a driver employing a sinusoidal drive voltage with a resonant energy recovery feature is typically employed. Such a driver is disclosed in U.S. Patent ~~Applications~~ Application No. 09/504,472 (now U.S. Patent No. 6,448,950) and U.S. Patent Application No. 10/036,002 (now U.S. Patent No. 6,819,308), the contents of which are incorporated herein by reference. However, it is nonetheless

desirable to tailor the output voltage for the gray levels to generate a gray scale response similar to that described by the empirical relation ship given by ~~equation~~ Equation 1.

According to the prior art, circuits are known for gray scale compensation in flat panel displays.

For example, U.S. Patent No. 5,652,600 (Khormaei et al) discloses a gray-scale correction system for EL displays which involves illuminating first selected pixel electrodes with data signals during a first subframe time period of the received image and thereafter energizing a second set of selected pixel electrodes with data signals during the next subframe time period where the first and second illumination signals have predetermined characteristics that differ from each other. The structure of the EL display is complex, and does not suggest the use of a reference voltage generator that employs a non-linear voltage ramp to generate gray-scale levels having correct luminance levels in an EL display.

U.S. Patent No. 5,812,104 (Kapoor et al) discloses the use of different levels of pixel luminance to achieve correct gray-scaling in an EL display. The '104 patent acknowledges the problem of prior art ramp generators to adequately vary the rate of the ramped voltage signal from a constant value throughout the ramp. In response to that, the '104 patent sets forth a gray-scale stepped ramp voltage generator constructed so that various step sizes may be obtained during each of the voltage steps. The disclosed circuit is very complex and is not capable of generating an intensity dynamic range of 256 x 256 (gamma = 2.0 per equation 1) between lowest and highest gray levels. Further, the use of TFEL devices is not amenable to achieving the gray levels to meet television standards, as set forth above.

U.S. Patent No. 6,417,825 (Stewart et al) discloses an EL display with gray-scale and a ramp voltage that may be made non-linear. However, the '825 patent is applicable only to active matrix EL and to frame rate modulation, not passive matrix EL and voltage modulation.

The following prior art is of background ~~interests~~ interest to the present invention:

U.S. Patent No. 5,227,863 (Bilbrey et al)

U.S. Patent 5,550,557 (Kapoor et al)

SUMMARY OF THE INVENTION

According to the present invention, Gamma correction of an EL panel is conveniently effected at the D/A conversion stage of a gray scale driver by replacing the conventional linear voltage ramp with a special 'double-inverted-S' non-linear voltage ramp.

Thus, a gray scale reference voltage generator is set forth herein that employs a non-linear voltage ramp in combination with a counter and a sample-and-hold circuit to achieve digital data to gray level conversion with proper Gamma correction.[[.]] The shape of the voltage ramp is defined to generate gray scale levels according to equation 1 taking into account the shape of the luminance versus voltage curve for a pixel, as shown in Figure 3 for a thick dielectric electroluminescent display. The optimum curve of the voltage ramp therefore has an inverted s-shape, with a convex shape (negative second derivative with respect to time) for an initial portion of the voltage range and a concave shape (positive second derivative with respect to time) for the remaining portion of the ramp to maximum luminance. The non-linear voltage ramp of the present invention permits the use of a clock that is required to delineate only 256 time intervals for fully defining 256 gray levels. The voltage ramp also simplifies the process of generating a Gamma corrected gray level voltage at the driver output in accordance with gray level data from the incoming video signal.

Other and further advantages and features of the invention will be apparent to those skilled in the art from the following detailed description thereof, taken in conjunction with the accompanying drawings introduced herein above.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to Figures 1, 2 and 3, and in contrast with the prior art, the present invention is optimized for use with an electroluminescent display having a thick film dielectric layer. A typical curve showing luminance versus driving voltage pulse amplitude for such a display is shown in Figure 3. Ideal gray level generating voltage ramp functions for positive and for negative row voltages generated for the luminance curve of Figure 3 are shown in Figure 4, as discussed in greater detail below.

As shown in the block diagram of Figure 6, the gray-scale circuit according to the present invention uses a non-linear voltage ramp to generate reference voltages to define specified gray levels on the columns, as discussed in greater detail below.

In operation, row electrodes are sequentially addressed to generate the complete frame image. As discussed above, voltages are applied essentially simultaneously to the columns of each addressed row to create the pixel luminosities required to generate the image for each frame. In order to eliminate time-averaged electric potential across any one pixel (a condition that shortens the life of a display due to degradation mechanisms associated with electric field assisted diffusion of chemical species in the pixel), the rows are addressed with alternating electric polarity. However, each of the display column drivers has a unipolar output, thereby necessitating a special addressing scheme.

Specifically, when a selected row is addressed with a negative row voltage, the magnitude of that voltage is equal to the threshold voltage so that no light is emitted from any pixel on that row unless there is an additive column voltage also applied to that pixel. When a selected row is addressed with a positive voltage, the magnitude of that voltage is equal to the voltage required for maximum luminance and voltages from the columns are subtracted from that voltage to achieve the desired gray level. These requirements must be reconciled with the use of a voltage ramp starting from zero volts to generate the gray scale reference voltages. The method of reconciliation according to the present invention is to convert the incoming digital 8 bit gray-scale digits to their complement values (i.e. replace binary zeros with ones and binary ones with zeroes) when the row voltage is positive so that the gray-scale level and the corresponding luminance level bear an inverse relation to one another.

This correction by itself, however, is insufficient to achieve gray scale fidelity, and the non-linear ramp function established for a negative row voltage must also be modified for use with a positive row voltage according to ~~equation~~ Equation 2 given by $V_{g\,pos.}(t) = V_m - V_{g\,neg}$ $(t_m - t)$ where $V_{g\,pos.}(t)$ is the ramp voltage as a function of the running time for the counter for positive row voltage and $V_{g\,neg}(t_m - t)$ is the established ramp voltage function for a negative row voltage expressed as a function of the difference between the time t_m for the ramp to reach the voltage value V_m for maximum luminance and the running time for the counter. Graphically, the two functions $V_{g\,pos.}(t)$ and $V_{g\,neg}(t)$ are rotated 180° with respect to one another. Thus, for the luminance versus voltage curve of Figure 3, both functions assume a convex shape (positive second derivative with respect to time) for the initial portion of the curve and a concave shape (negative second derivative with respect to time) for the remaining portion of the curve to a maximum value of $t = t_m$. The two functions derived for the luminance curve of Figure 3 are shown in Figure 4.

There are various techniques that can be used to generate the appropriate non-linear voltage ramp functions $V_{g\,pos.}(t)$ and $V_{g\,neg}(t)$. According to the preferred embodiment of Figure 6, two time-dependent voltage feedback controlled current sources (I-1 and I-2 circuits) are used to generate the two segments of the non-linear ramp. The I-1 current source has a current magnitude that decreases with time, and the I-2 current source has a magnitude that increases with time. By controlling the proper timing of switching between the two current sources, as determined by the Threshold Control Circuit, and by directing the currents to an Integrator Circuit, an approximation to the voltage ramp curve of Figure 4 is generated.

The output of the Integrator Circuit is applied to the conventional Column Driver comprising a counter and Sample-and-Hold (S/H) circuit.

The shape of the generated non-linear ramp voltage can be adjusted or fine-tuned for a particular panel characteristic by altering the functional parameters of the current sources, as discussed in greater detail below with reference to Figure 7.

In addition, a Frame Polarity Control Circuit is included in the ramp generator to select between the two ramp curves for positive and negative row voltages / frames.

Closer approximations to the curves of Figure 4 or similar curves for displays having different luminance versus applied voltage characteristics can be generated using three or more current sources with different time-dependent functions selected sequentially in proper timing and sequence, or connected in various parallel combinations.

A simplified alternative to the preferred embodiment of Figure 6 is to substitute the two time-dependent variable current sources with two constant (time-independent) current sources. This results in a stepwise ramp curve similar to that of Figure 5. While more simple in design, the stepwise ramp provides gray scale correction with degraded performance as compared to the double-inverted-S ramp of Figure 4.

A successful prototype of the Double-inverted-S Ramp Generator is shown in Figure 7. The dashed line blocks represent circuitry that provide the functionality of the blocks in Figure 6. This circuit also includes control inputs for independent adjustments of three critical parameters for each of the non-linear ramps for both negative and positive row polarities, and also the timing for automatic switching between the two non-linear ramps as controlled by the frame polarity synchronization pulse from the display system. The three critical parameters are the curvature of the first segment of the non-linear ramp (adjusted through R15 and R16 of Figure 7), the transition voltage level for switching between the two non-linear ramp segments (adjusted through R9 and R10 of Figure 7), and the curvature of the second segment of the non-linear ramp (adjusted through R5 and R6 of Figure 7). A ramp reset signal derived from the system control electronics is used to reset and synchronize the non-linear ramp for every scan cycle of the display.

The procedure for the adjustment and optimization of the non-linear ramp for each display panel is first to generate the luminance versus gray-level characteristic of a particular panel using the conventional single linear ramp. An ideal characteristic curve is then derived based on ~~equation~~ Equation 1 and the luminance of the panel at the maximum gray level.

With the assumed value of 2 assigned to α in ~~equation~~ Equation 1, the appropriate value of 'A' can be generated by trial and error (for example using Microsoft EXCEL software). With the one-to-one mapping between the panel characteristic curve and the ideal characteristic curve, an ideal shape of the non-linear ramp can be generated. The three critical parameters of the non-linear ramp are adjusted based on the generated calculated ideal ramp.

A gray-scale correcting circuit was built for a 17 inch 480 by 640 pixel VGA format diagonal thick film colour electroluminescent display using Hitachi ECN2103 row drivers and Supertex HV623 column drivers. Each pixel had independent red, green and blue sub-pixels addressed through separate columns and a common row. The threshold voltage for each of the red, green and blue sub-pixels of this display was 140 volts. The circuit was used in conjunction with an energy recovery resonant sine-wave drive circuit with a compensating circuit to eliminate gray level variations due to the variable capacitive impedance of the panel as exemplified in ~~US patent applications 09/504472 and 10/036002.~~ above-mentioned and incorporated U.S. Patent Nos. 6,448,950 and 6,819,308.

Figure 8 shows the relationship between luminance and gray-level number for the successful prototype 17" display with a conventional single linear ramp compared to one with the non-linear ramps for positive and for negative row voltages of the instant invention. An ideal characteristic curve is also provided for comparison. The characteristic curve generated using the non-linear ramps shows very close proximity to the ideal characteristic.

Although multiple specific embodiments of the invention have been described herein, it will be understood by those skilled in the art that variations may be made thereto without departing from the spirit of the invention or the scope of the appended claims.